## REMARKS

Claims 1-4, 7-17, 19 and 22-26 are pending in this application. By this Response, claims 5-6 and 18 are canceled, claims 1, 10, 22, and 23 are amended, and claims 24-26 are added. Claims 1, 10, 22, and 23 are amended to recite that a high low clock pulse shuttle circuit/shuttle node provides an unconditioned clock signal/clock pulse to a block delay module when the clock pulse width is outside a clock pulse width limit and the high low clock pulse shuttle circuit/shuttle node is bypassed when the clock pulse width is equal to or less than the clock pulse width limit. Support for these amendments may be found at least in Figure 4 and at pages 13-15 of the present specification. No new matter has been added by the amendment to claim 23 above. Reconsideration of the claims in view of the above amendments and the following remarks is respectfully requested.

### I. Status of Office Action

The Office Action mailed October 20, 2006 was indicated as being a Final Office Action alleging that the change in the grounds of rejection were necessitated by Applicants' amendment. However, as explained to the Examiner in a telephone interview conducted on November 7, 2006, the amendments to the claims were only to incorporate subject matter that the Examiner indicated to be allowable and thus, the change in grounds of rejection was not necessitated by Applicants' amendments. Moreover, claims 10-19 were not amended (with the exception of claim 11 which was amended to correct its dependency) and thus, the change in grounds of rejection for these claims could not possibly be based on any amendment made by Applicants. In response, Examiner Almo agreed that the October 20, 2006 Office Action should not have been made final and that the finality of the Office Action would be withdrawn. Examiner Almo indicated that a communication would be mailed specifically stating that the October 20, 2006 Office Action is a Non-Final Office Action, however as of the filing of this Response, no such communication has been received. However, it is Applicants' understanding that the Examiner is in agreement that the October 20, 2006 Office Action is Non-Final and thus, the finality indicated in the Office Action has been withdrawn.

## II. Rejection under 35 U.S.C. § 103(a)

The Office Action rejects claims 1-19 and 22-23 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Sher (U.S. Patent Application Publication No. 2001/0011913) in view of Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Prentice Hall, 1996, Chapter 4, page 193[1]. This rejection is respectfully traversed.

Independent claim 1 reads as follows:

> 1. A pulse width limiting circuit, comprising:
>
> a clock signal correction block configured to receive a conditioned clock signal and generate a corrected clock output signal, wherein the clock signal comprises a train of clock pulses, each of which has a rising clock edge, a falling clock edge and a variable width;
>
> a block delay module, coupled to the clock signal correction block, configured to accept an unconditioned clock signal and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay; and
>
> a high low clock pulse shuttle circuit, coupled to the clock signal correction block, configured to accept the conditioned clock signal, wherein the high low clock pulse shuttle comprises a first field effect transistor (FET) coupled to the correction block and a second FET coupled to a conditioned clock signal output interconnect, and wherein the high low clock pulse shuttle circuit shunts the unconditioned clock signal to the block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit, and wherein the unconditioned clock signal is passed as the corrected clock output signal if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing the high low clock pulse shuttle circuit.
> (emphasis added)

Applicants respectfully submit that neither Sher nor Rabaey, either alone or in combination, teach or suggest at least those features of claim 1 emphasized above.

Sher is directed to a circuit for generating an internal clock signal even under extreme temperature and supply voltage variations. The circuit of Sher is shown in

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[1] Although the statement of the rejection only mentions the Sher reference, the body of the rejection of claim 1 references the Rabaey reference and thus, it is Applicants' understanding that all of the claims are rejected based on an alleged combination of Sher and Rabaey.

Figure 2 of Sher. As shown in Figure 2, an unconditioned clock signal X CLK is input to an inverter 3 which inverts the unconditioned clock signal to generate an inverted clock signal X*. The inverted clock signal X* is input to NAND gates 5 and 11 which constitute a Set-Reset (SR) flip-flop 45. The SR flip-flop 45 provides an output to inverter 13 of the switching circuit 47 which inverts the output of the SR flip-flop 45 to output a conditioned internal clock signal CLK Y. The inputs of the second NAND gate 11 of the SR flip-flop 45 are driven high or pulled low by the transistors 7, 9, and 27 of the trailing edge feedback path 49. The output of the inverter 13 in the switching circuit 47 is pulled low by the transistor 19. The delay element 23 in the trailing edge feedback path 49 introduces a delay into the output to the transistor 27 for pulling the input to the second NAND gate 11 of the SR flip-flop 45 low.

The circuit in Sher essentially delays the trailing edge of a clock input signal X CLK by a delay amount set forth in the delay element 23 when the clock input signal X is in a high state for greater than the delay amount. That is, the trailing edge feedback path 49 pulls the clock output signal CLK Y low after the delay amount.

While Sher limits the time period by which the X CLK signal is allowed to remain high, Sher does not teach or suggest the high low clock pulse shuttle circuit recited in claim 1. Moreover, Sher does not teach or suggest a high low clock pulse shuttle circuit shunts an unconditioned clock signal to a block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit. Furthermore, Sher does not teach or suggest that an unconditioned clock signal is passed as a corrected clock output signal if a clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit by bypassing a high low clock pulse shuttle circuit, as recited in claim 1.

The Office Action alleges that Sher teaches the high low clock pulse shuttle circuit as NAND gate 11 (see page 2 of the Office Action). NAND gate 11 receives the output from NAND gate 5 and the output from node D in the Sher's circuit and outputs a clock signal to inverter 13 which inverts the signal and outputs it as the internal clock signal CLK Y. The NAND gate 11 does not shunt an unconditioned clock signal to a block delay module if a clock pulse width of the unconditioned clock signal is outside a pulse width limit. To the contrary, the output of the inverter 13, and thus, the output of

the NAND gate 11, is always provided to the delay circuit 23 whose input, via the inverter 21, is the inverted internal clock signal CLK Y. Thus, NAND gate 11 does not provide any ability to shunt an unconditioned clock signal to a block delay module if the clock pulse width of the unconditioned clock signal is outside a pulse width limit.

Moreover, the NAND gate 11 of Sher does not pass an unconditioned clock signal through as a corrected clock output signal by bypassing a high low clock pulse shuttle circuit if the clock pulse width of the unconditioned clock signal is equal to or less than the pulse width limit. There is no ability in the circuit of Sher to bypass the NAND gate 11 when generating the clock output CLK Y. Thus, there is no ability in Sher to bypass the NAND gate 11 if a clock pulse width of the unconditioned clock signal is equal to or less than a pulse width limit.

The Rabaey reference is cited as teaching the internal elements of a NAND gate. While Rabaey teaches that a NAND gate may include an arrangement of transistor elements, as shown in Figure 4.3 of Rabaey, there is no teaching or suggestion in Rabaey to provide a high low clock pulse shuttle circuit such as that recited in claim 1. Thus, since neither reference, either alone or in combination, teaches or suggests the high low clock pulse shuttle circuit of claim 1, any alleged combination of the cited references still would not result in this feature being taught or suggested. Moreover, since neither reference teaches or suggests to bypass such a high low clock pulse shuttle circuit if a pulse width of an unconditioned clock signal is equal to or less than a pulse width limit, any alleged combination of the cited references still would not result in this feature being taught or suggested.

Similar distinctions of the claims over the cited references apply to independent claims 10, 22, and 23. Claim 10 recites "injecting the clock pulse through a block delay module in response to the clock shuttle node identifying a clock pulse width of the clock pulse as being outside a predetermined pulse width limit...substantially passing through the clock pulse by bypassing the clock shuttle node in response to the clock pulse width of the clock pulse being less than or equal to the predetermined pulse width limit" (emphasis added). Again, neither Sher nor Rabaey teach or suggest a clock shuttle node, let alone injecting a clock pulse through a block delay module in response to the clock shuttle node identifying a clock pulse width of the clock pulse being outside a

predetermined pulse width limit or bypassing the clock shuttle node in response to the clock pulse width of the clock pulse being less than or equal to the predetermined pulse width limit. Claims 22 and 23 recite features similar to that argued above with regard to claim 1 and thus, are distinguished over the alleged combination of references for similar reasons as set forth above with regard to claim 1.

Thus, Applicants respectfully submit that neither Sher nor Rabaey, either alone or in combination, teach or suggest the features of independent claims 1, 10, 22 and 23. At least by virtue of their dependency on claims 1 and 10, respectively, neither Sher nor Rabaey, either alone or in combination, teach or suggest the features of dependent claims 2-4, 7-9, and 11-19. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-19 and 22-23 under 35 U.S.C. § 103(a).

In addition to the above, dependent claims 2-4, 7-9, and 11-19 recite additional features which, when taken alone or in combination with the features of the independent claims from which they depend, are not taught or suggested by the cited references. For example, with regard to claim 3, neither reference teaches or suggests that a clock signal correction block provides a conditioned signal to a high low clock pulse shuttle circuit. Moreover, neither reference teaches or suggests a leak detector. The NAND gate 11 in Sher does not receive a conditioned clock signal from elements 3, 5, 7, 9 and 27, which the Office Action equates with the clock signal correction block. Moreover, element 3 in Sher is not a leak detector but rather simply an inverter.

As a further example, claim 7 recites a node to transmit the conditioned clock pulse between the clock signal correction block, the high low clock pulse shuttle circuit and a clock pulse inverter. The Office Action alleges that the "node Y" is equivalent to the node recited in claim 7. "Y" in Sher denotes the output of the second NAND gate 11 which is fed back to the first NAND gate 5. The output sent along this wire is not a conditioned clock signal that is provided to a high low clock pulse shuttle circuit (which the Office Action alleges is equivalent to NAND gate 11). The only inputs to the NAND gate 11 are the output of the first NAND gate 5 and the output from node D. The signal along "node Y" is not input to the NAND gate 11.

The other dependent claims recite other features which, when taken alone or in combination with the features of their respective independent claims, are not taught or

suggested by the alleged combination of references. Thus, in addition to being dependent upon their respective independent claims, dependent claims 2-4, 7-9, and 11-19 are also distinguished over the alleged combination of references by virtue of the specific features recited therein.

## III. Newly Added Claims

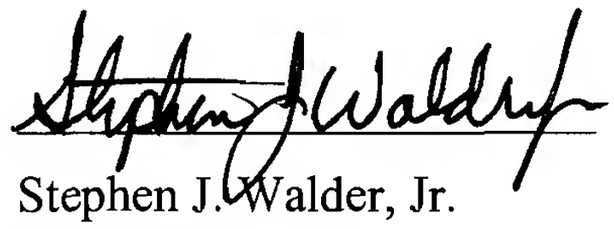
Claims 24-26 are added to recite additional features of the present invention. The features of claims 24-26 are supported at least by Figure 4 and the description on pages 13-15 of the present specification. No new matter has been added by the addition of claims 24-26. Prompt and favorable consideration of claims 24-26 is respectfully requested.

## IV. Conclusion

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

DATE: January 19, 2007



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